FIG.1

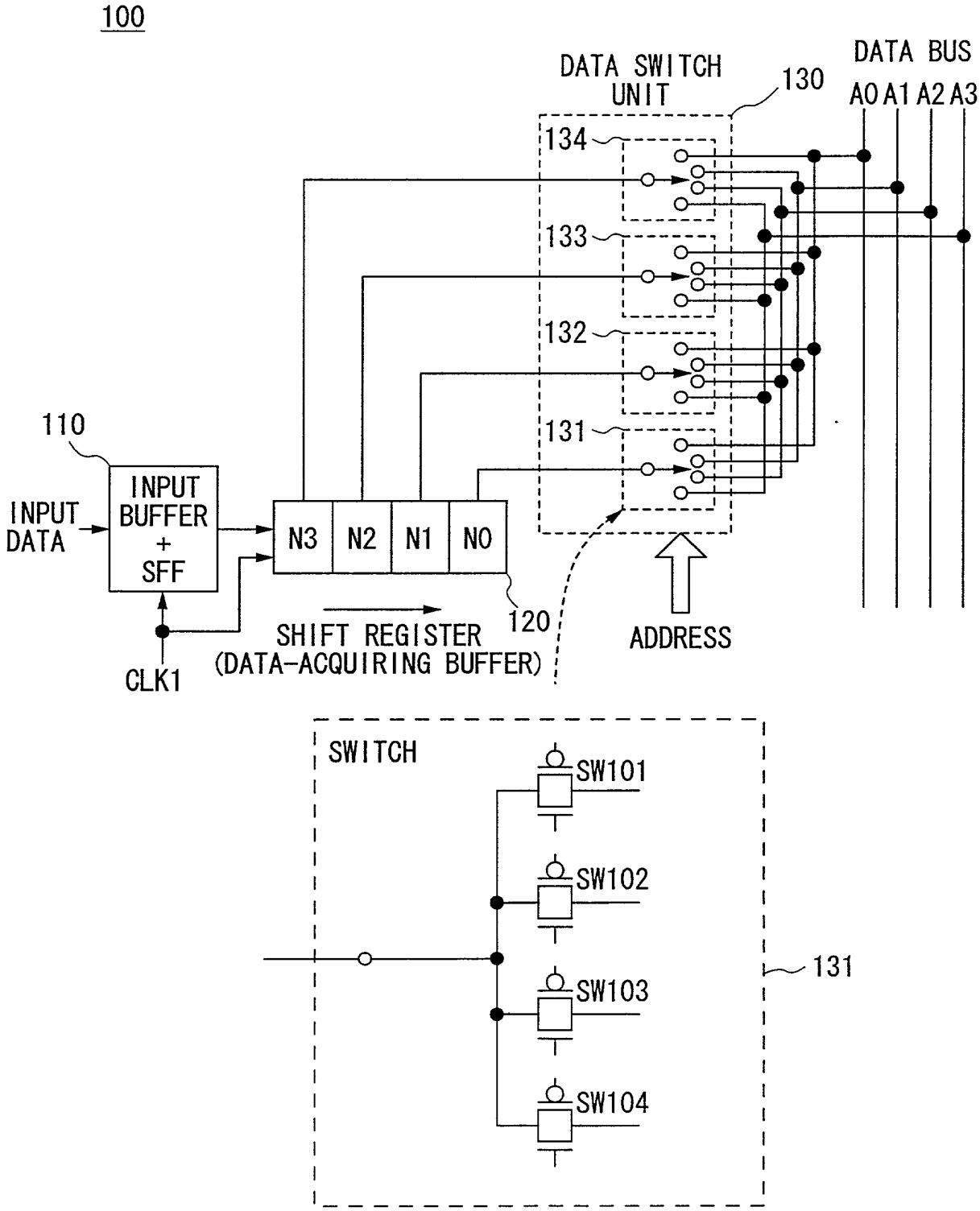

100
DATA SWITCH UNIT
130
DATA BUS
A0 A1 A2 A3
134
133
132
131
110
INPUT DATA
INPUT BUFFER + SFF
N3
N2
N1
N0
120
SHIFT REGISTER (DATA-ACQUIRING BUFFER)
ADDRESS
CLK1
SWITCH
SW101
SW102
SW103
SW104
131

FIG.2A

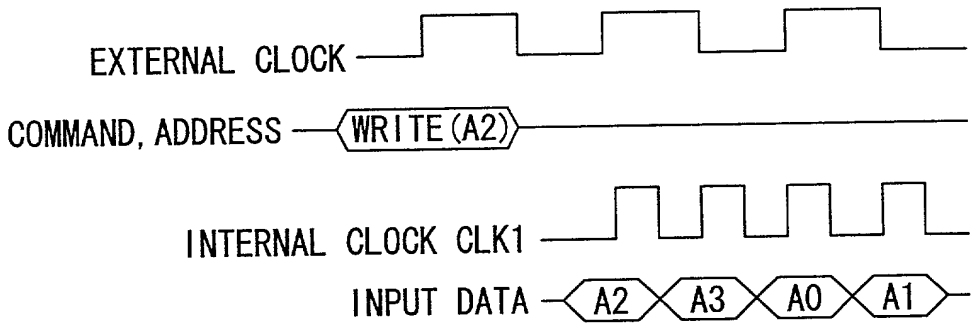
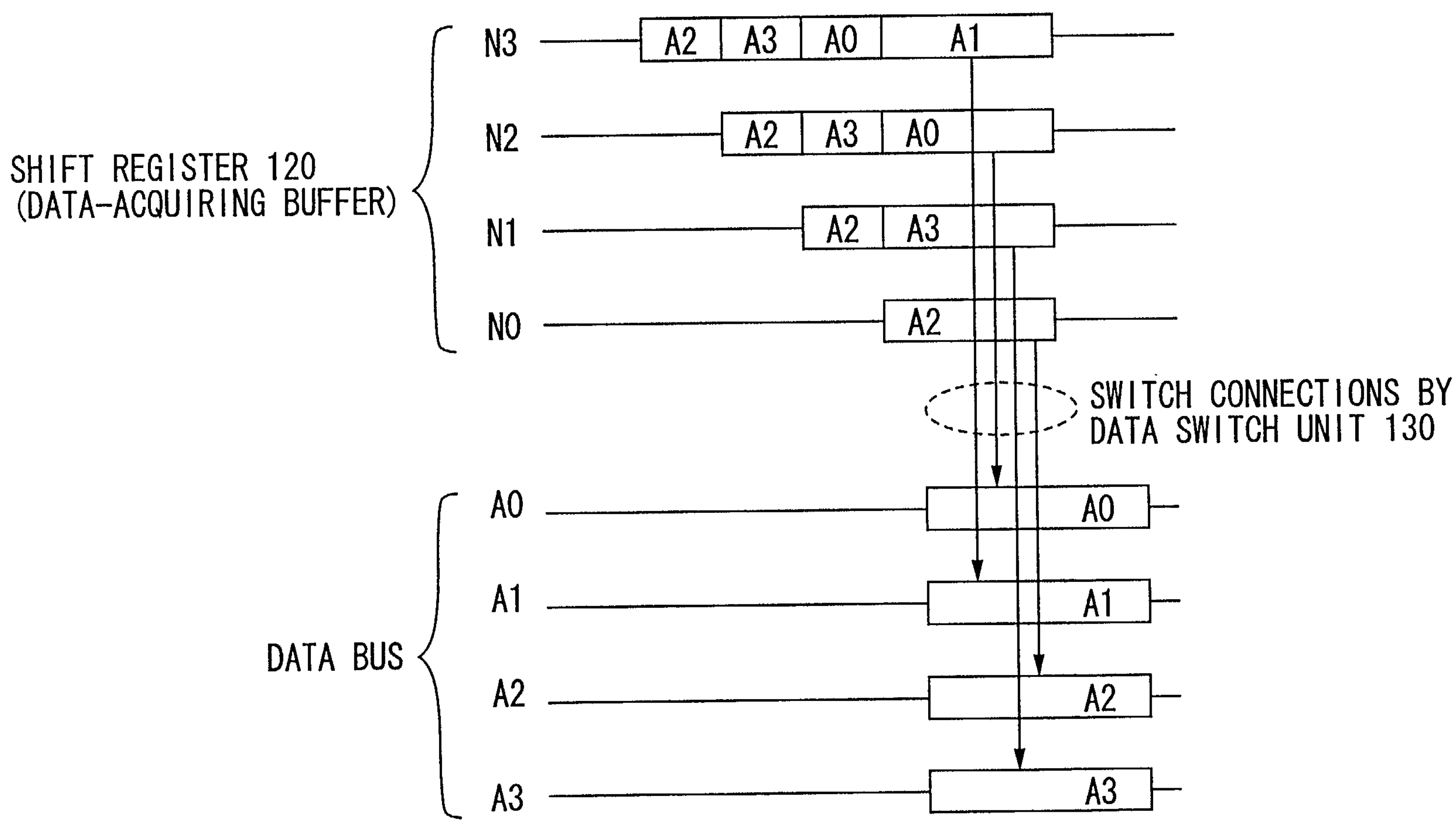

EXTERNAL CLOCK
COMMAND, ADDRESS
WRITE(A2)
INTERNAL CLOCK CLK1
INPUT DATA
A2
A3
A0
A1

FIG.2B



SHIFT REGISTER 120
(DATA-ACQUIRING BUFFER)
N3
N2
N1
N0
A2
A3
A0
A1
SWITCH CONNECTIONS BY
DATA SWITCH UNIT 130
DATA BUS

FIG.3

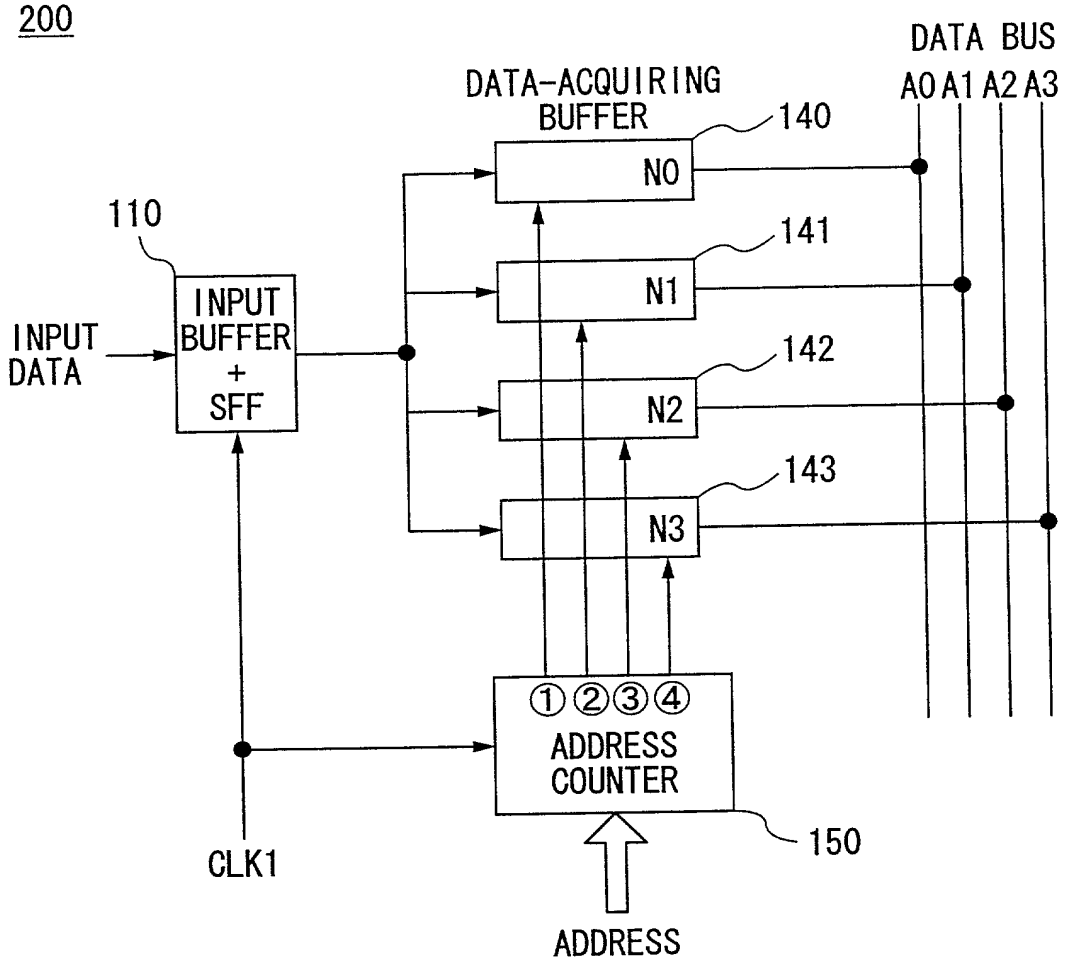

200
DATA BUS
A0 A1 A2 A3
DATA-ACQUIRING BUFFER
140
N0
141
N1
142
N2
143
N3
110
INPUT BUFFER + SFF
INPUT DATA
①②③④
ADDRESS COUNTER
150
CLK1
ADDRESS

FIG.4A

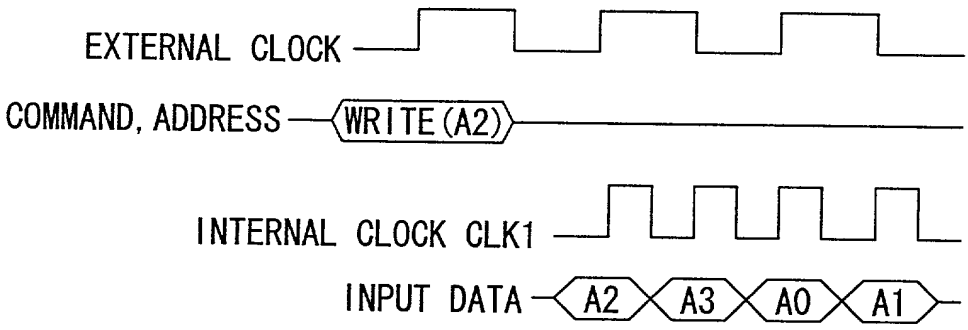

EXTERNAL CLOCK
COMMAND, ADDRESS
WRITE(A2)
INTERNAL CLOCK CLK1
INPUT DATA
A2
A3
A0
A1

FIG.4B

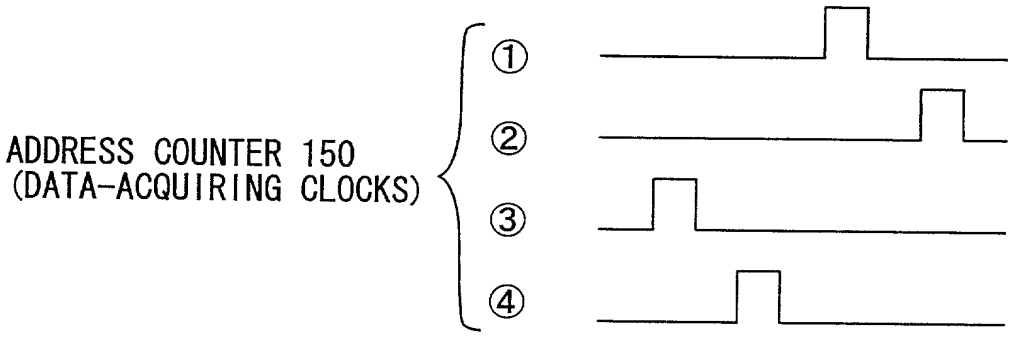

ADDRESS COUNTER 150
(DATA-ACQUIRING CLOCKS)
①
②
③
④

FIG.4C

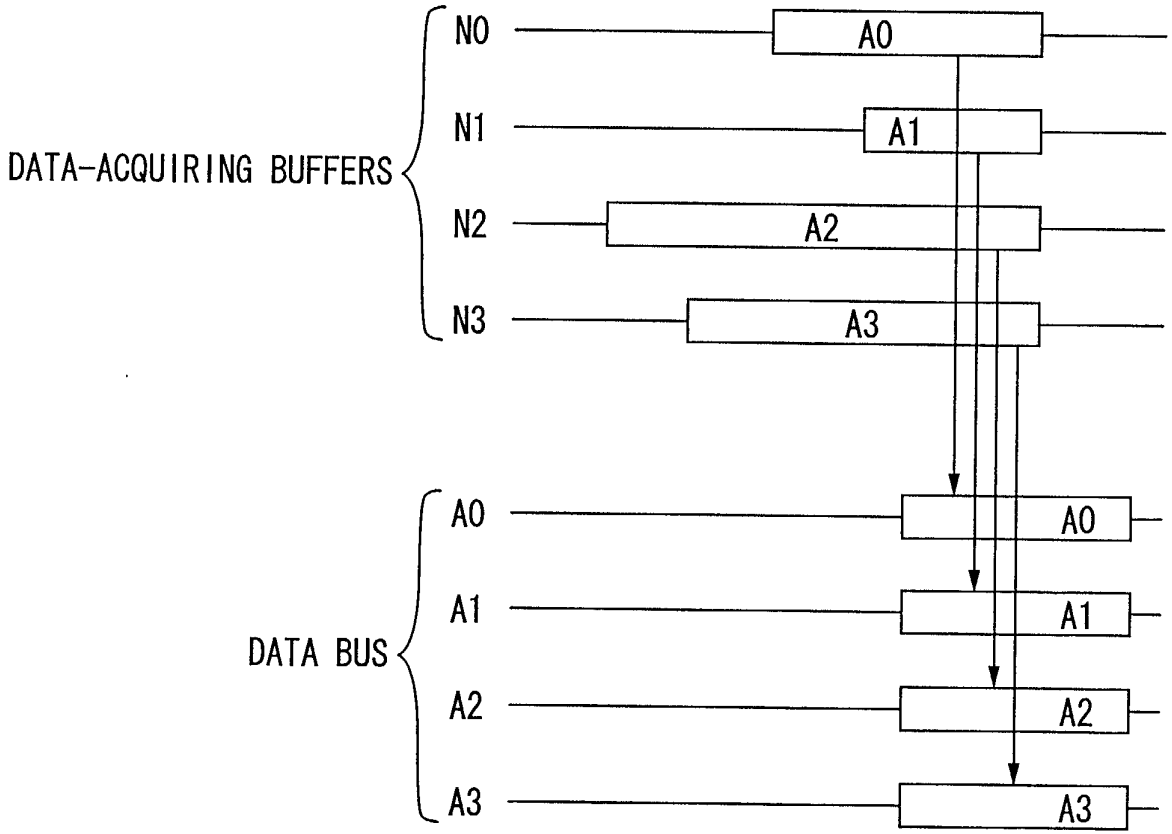

DATA-ACQUIRING BUFFERS
N0
N1
N2
N3
A0
A1
A2
A3
DATA BUS
A0
A1
A2
A3
A0
A1
A2
A3

FIG.5

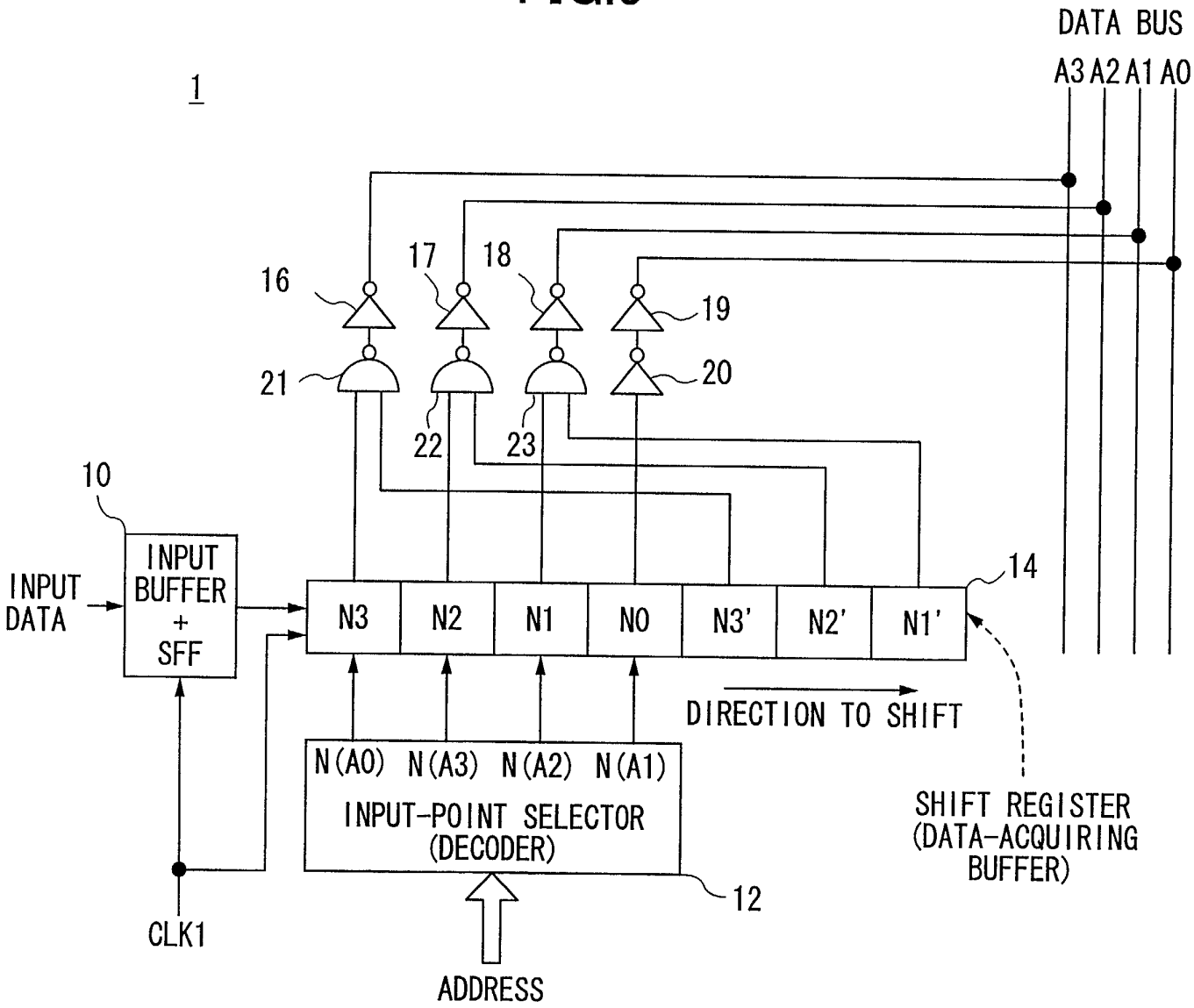

DATA BUS
A3 A2 A1 A0
1
16
17
18
19
21
20
22
23
10
INPUT DATA
INPUT BUFFER + SFF
N3
N2
N1
N0
N3'
N2'
N1'
14
DIRECTION TO SHIFT
N(A0) N(A3) N(A2) N(A1)
INPUT-POINT SELECTOR (DECODER)
12
SHIFT REGISTER (DATA-ACQUIRING BUFFER)
CLK1
ADDRESS

FIG.6A

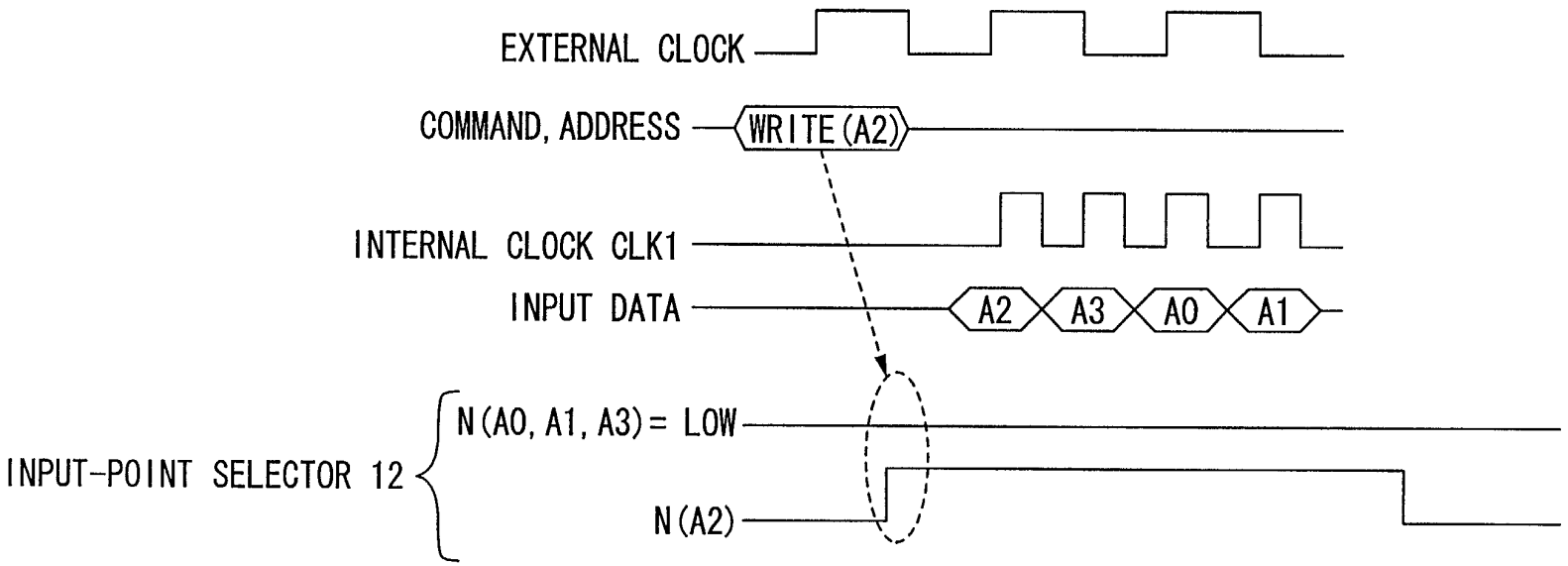

EXTERNAL CLOCK
COMMAND, ADDRESS
WRITE(A2)
INTERNAL CLOCK CLK1
INPUT DATA
A2
A3
A0
A1
INPUT-POINT SELECTOR 12
N(A0, A1, A3) = LOW
N(A2)

FIG.6B

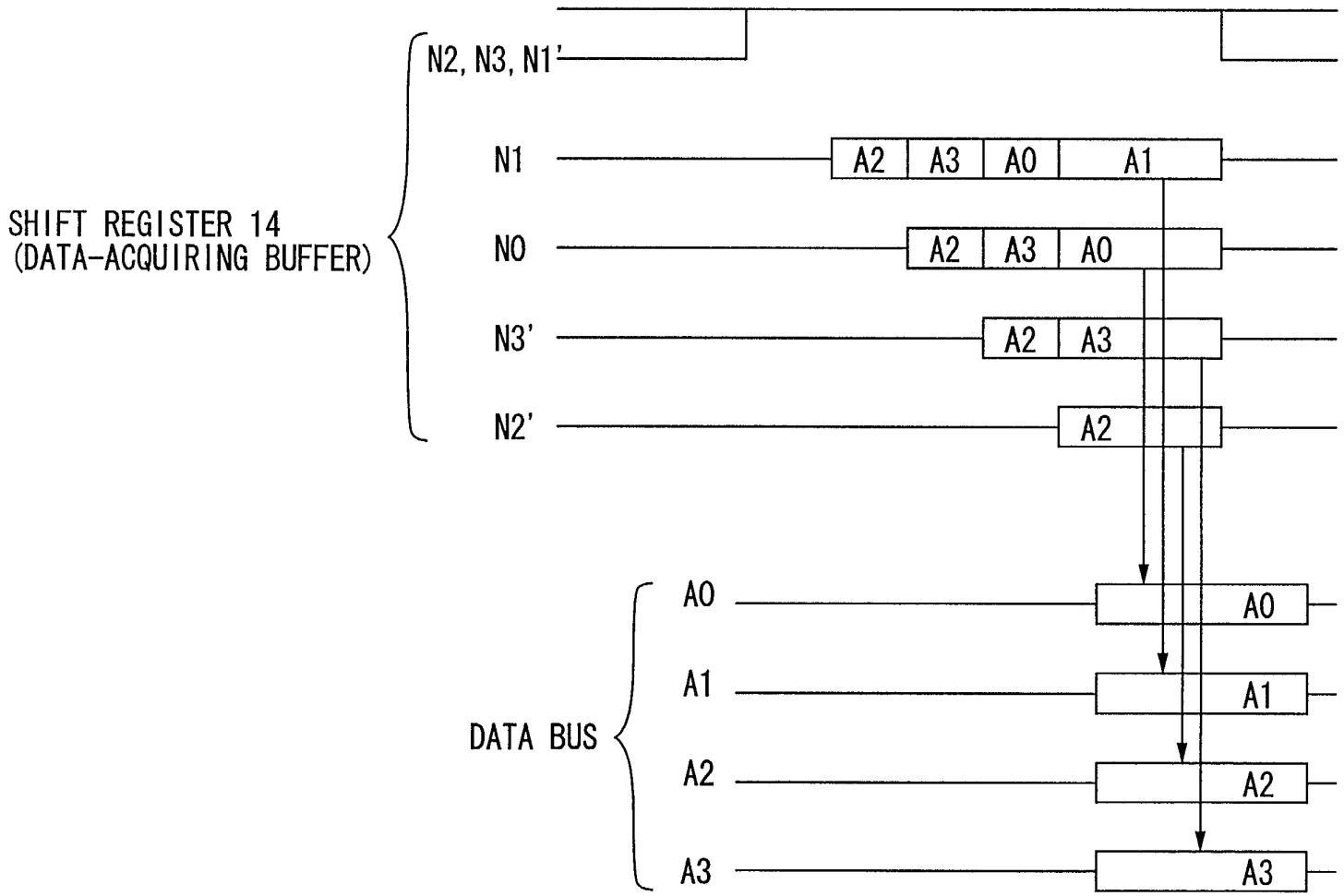

N2, N3, N1'
N1
N0
N3'
N2'
SHIFT REGISTER 14
(DATA-ACQUIRING BUFFER)
A2
A3
A0
A1
A2
A3
A0
A2
A3
A2
A0
A1
A2
A3
DATA BUS
A0
A1
A2
A3

FIG.7

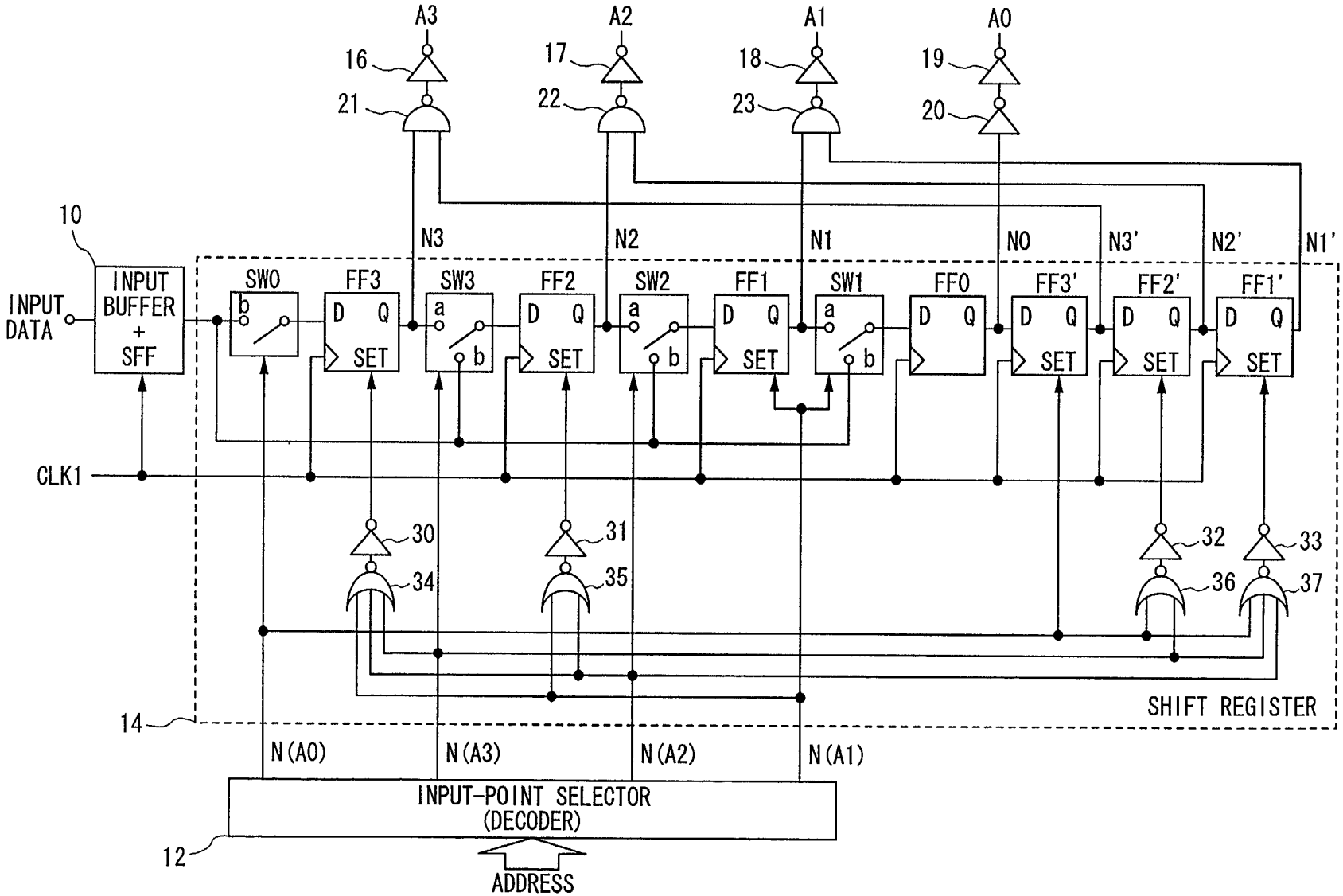

A3
A2
A1
A0
16
17
18
19
21
22
23
20
10
N3
N2
N1
NO
N3'
N2'
N1'
INPUT DATA
INPUT BUFFER + SFF
SW0
SW3
SW2
SW1
FF3
FF2
FF1
FF0
FF3'
FF2'
FF1'
D Q
SET
a
b
CLK1
30
31
32
33
34
35
36
37
14
SHIFT REGISTER
N(A0)
N(A3)
N(A2)
N(A1)
INPUT-POINT SELECTOR (DECODER)
12
ADDRESS

FIG.8

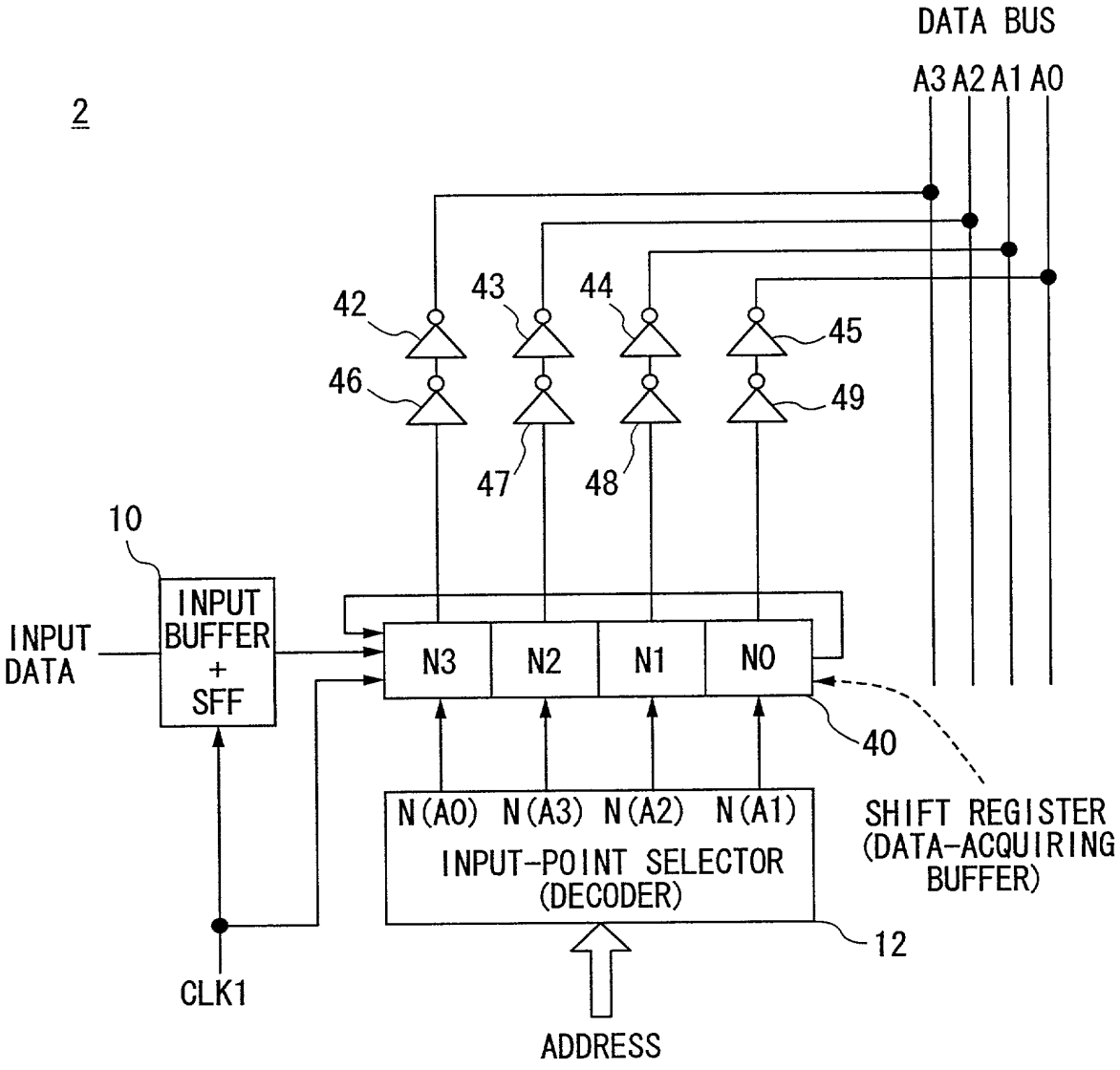

DATA BUS
A3 A2 A1 A0
2
42
43
44
45
46
47
48
49
10
INPUT BUFFER + SFF
INPUT DATA
N3
N2
N1
N0
40
SHIFT REGISTER (DATA-ACQUIRING BUFFER)
N(A0) N(A3) N(A2) N(A1)
INPUT-POINT SELECTOR (DECODER)
12
CLK1
ADDRESS

FIG.9A

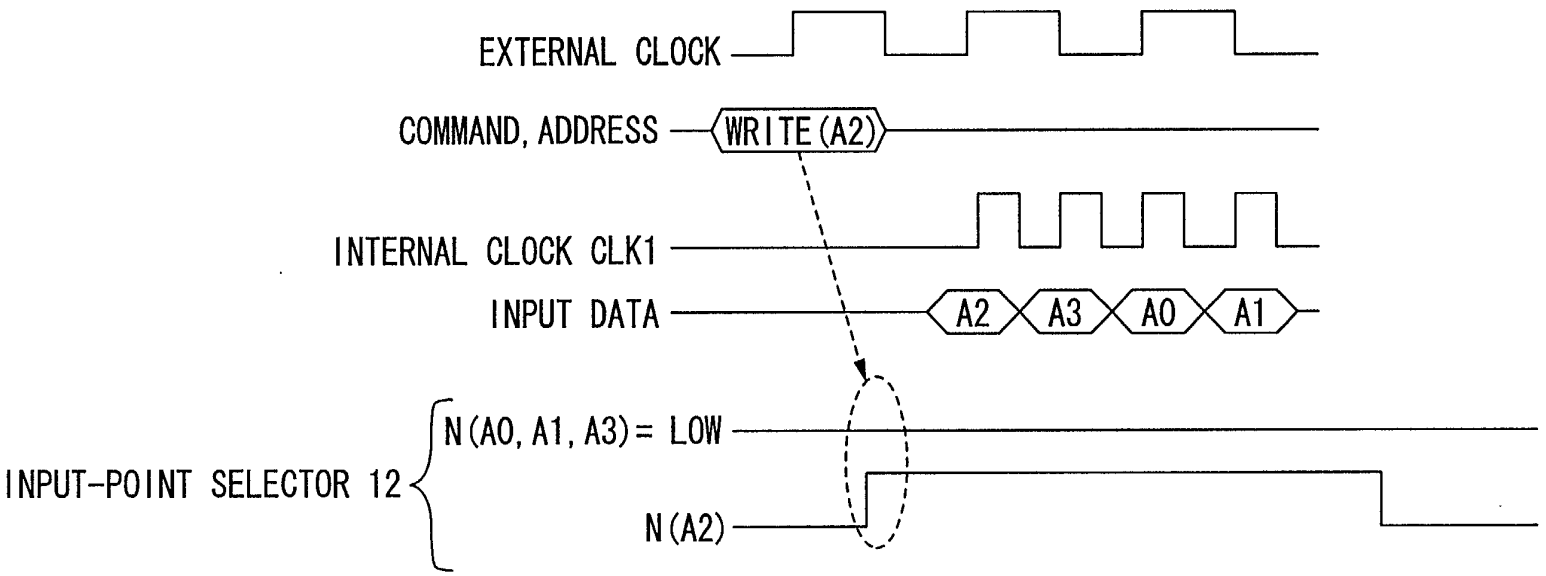

EXTERNAL CLOCK
COMMAND, ADDRESS
WRITE(A2)
INTERNAL CLOCK CLK1
INPUT DATA
A2
A3
A0
A1
INPUT-POINT SELECTOR 12
N(A0, A1, A3)= LOW
N(A2)

FIG.9B

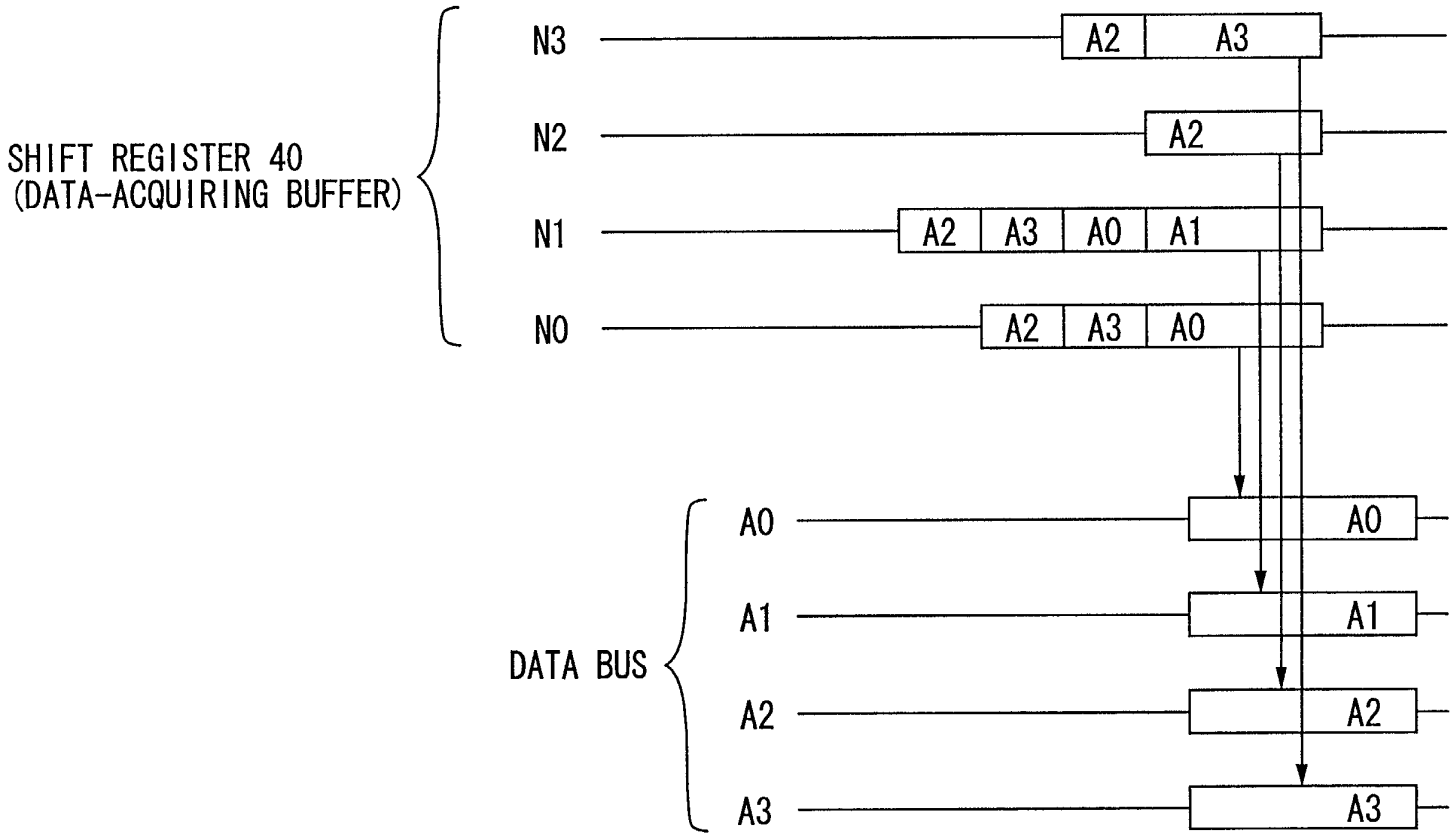

SHIFT REGISTER 40
(DATA-ACQUIRING BUFFER)
N3
N2
N1
N0
A2
A3
A0
A1
DATA BUS
A0
A1
A2
A3

FIG.10

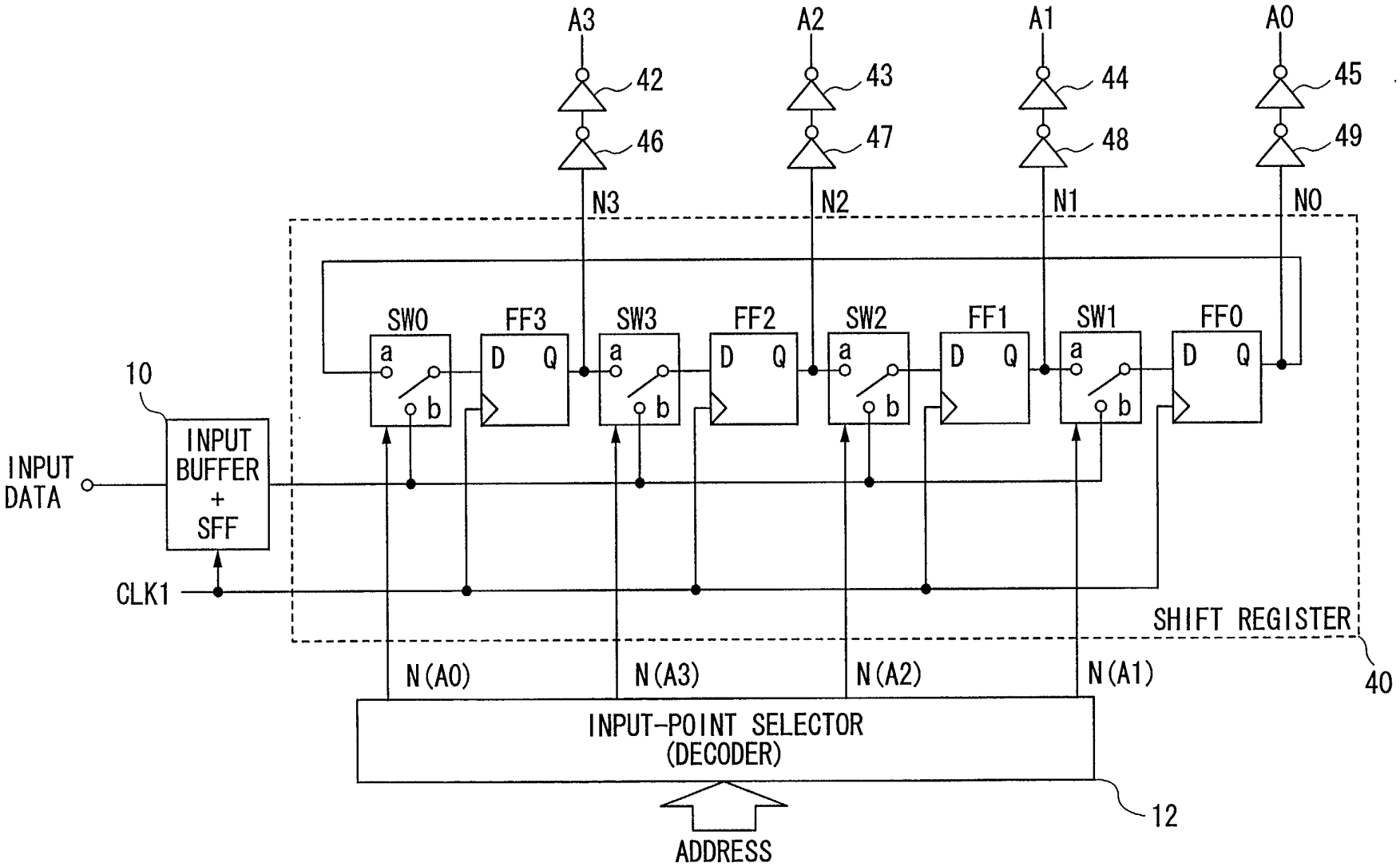
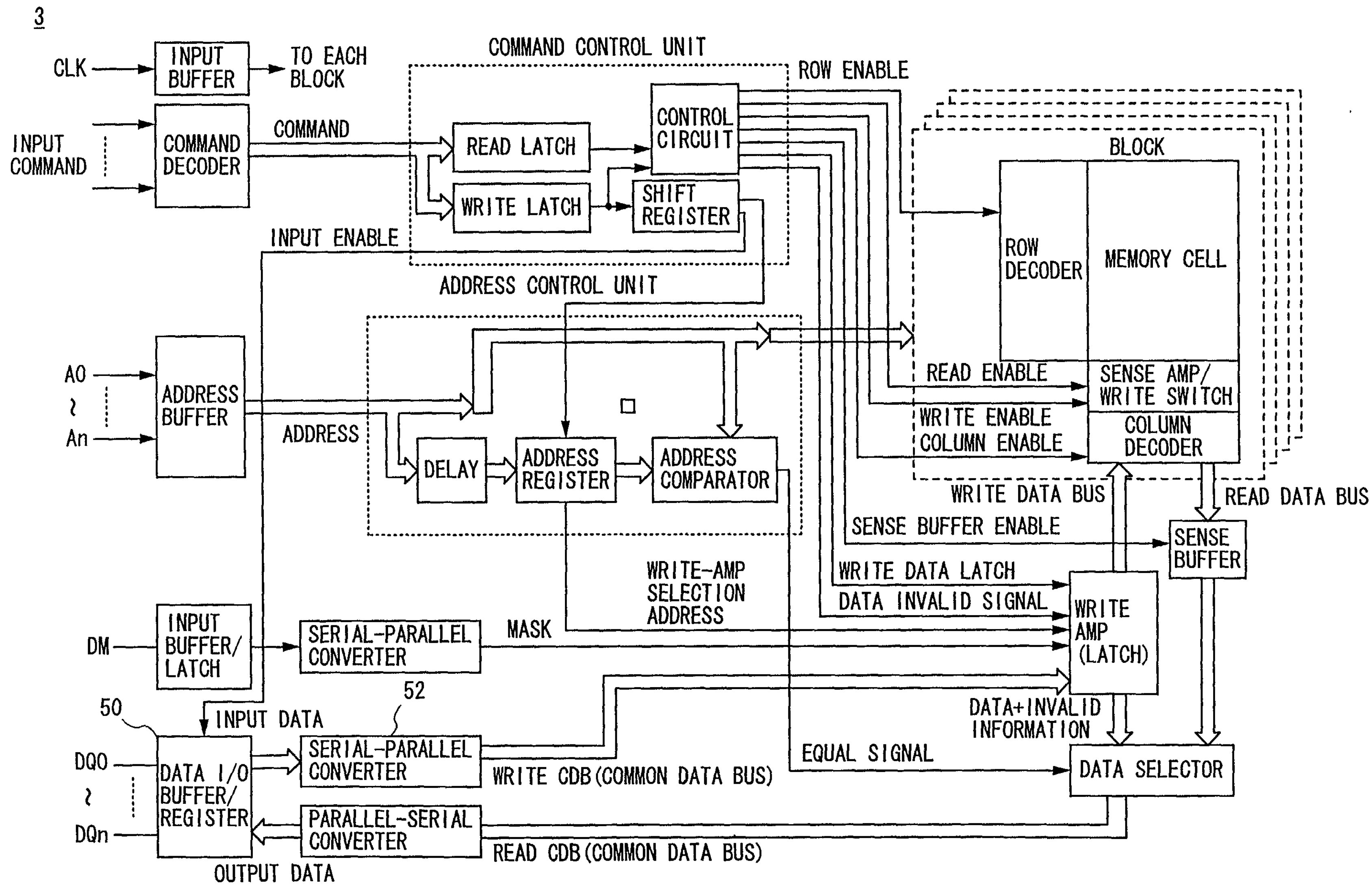

A3
A2
A1
A0
42
43
44
45
46
47
48
49
N3
N2
N1
N0
SW0
FF3
SW3
FF2
SW2
FF1
SW1
FF0
a
b
D
Q
10
INPUT BUFFER + SFF
INPUT DATA
CLK1
SHIFT REGISTER
40
N(A0)
N(A3)
N(A2)
N(A1)
INPUT-POINT SELECTOR (DECODER)
12
ADDRESS

FIG.11


3
CLK
INPUT BUFFER
TO EACH BLOCK
INPUT COMMAND
COMMAND DECODER
COMMAND
COMMAND CONTROL UNIT
READ LATCH
WRITE LATCH
CONTROL CIRCUIT
SHIFT REGISTER
ROW ENABLE
BLOCK
ROW DECODER
MEMORY CELL
SENSE AMP/ WRITE SWITCH
COLUMN DECODER
INPUT ENABLE
ADDRESS CONTROL UNIT
A0 ~ An
ADDRESS BUFFER
ADDRESS
DELAY
ADDRESS REGISTER
ADDRESS COMPARATOR
READ ENABLE
WRITE ENABLE
COLUMN ENABLE
WRITE DATA BUS
READ DATA BUS
SENSE BUFFER ENABLE
SENSE BUFFER
WRITE DATA LATCH
DATA INVALID SIGNAL
WRITE-AMP SELECTION ADDRESS
WRITE AMP (LATCH)
DM
INPUT BUFFER/ LATCH
SERIAL-PARALLEL CONVERTER
MASK
50
52
INPUT DATA
DQ0 ~ DQn
DATA I/O BUFFER/ REGISTER
SERIAL-PARALLEL CONVERTER
WRITE CDB (COMMON DATA BUS)
DATA+INVALID INFORMATION
EQUAL SIGNAL
DATA SELECTOR
PARALLEL-SERIAL CONVERTER
READ CDB (COMMON DATA BUS)
OUTPUT DATA